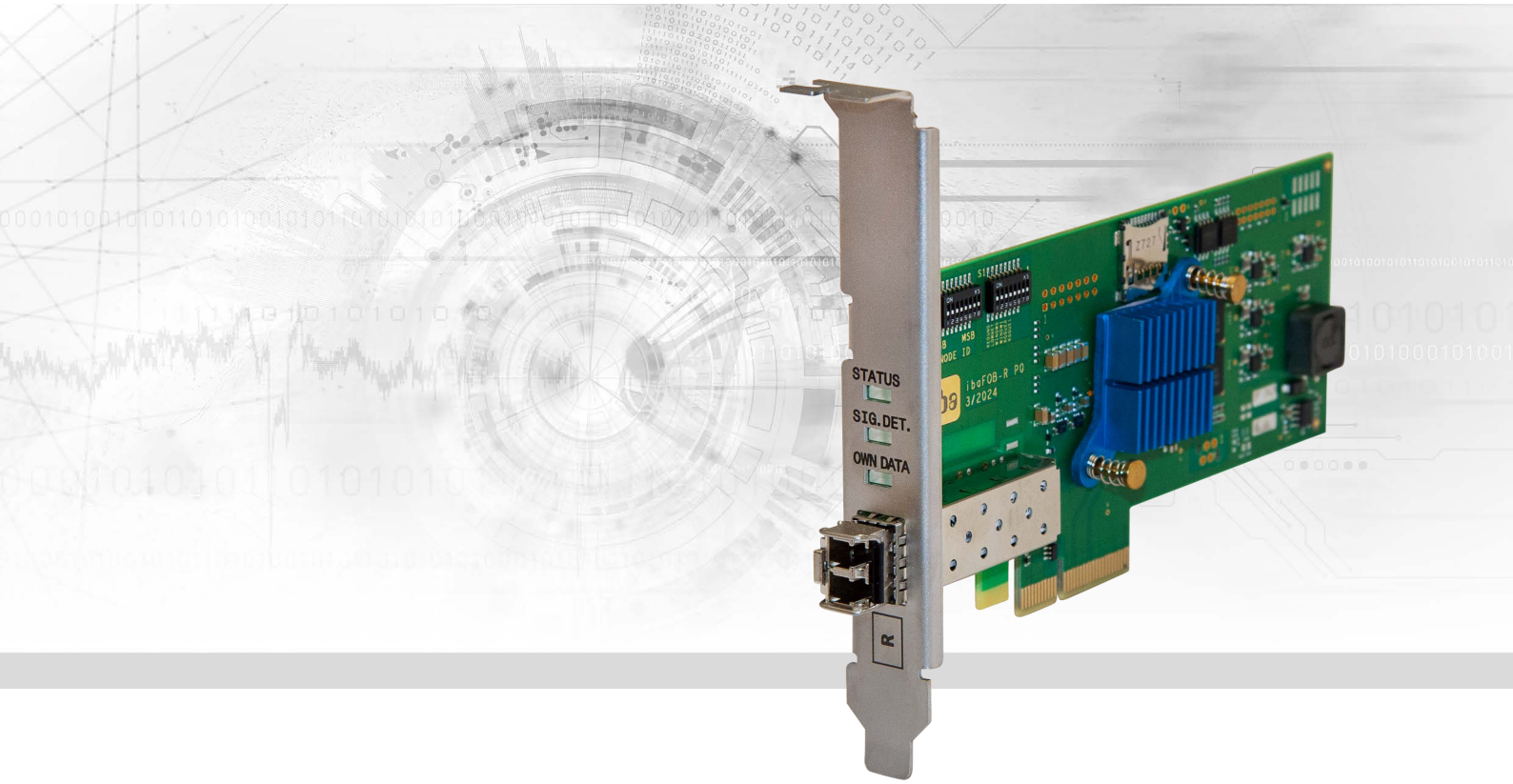


ibaFOB-R

Reflective Memory Interface Board

Manual

Issue1.0

Measurement Systems for Industry and Energy

www.iba-ag.com

Manufacturer

iba AG

Koenigswarterstraße 44

90762 Fuerth

Germany

Contacts

Headquarters	+49 911 97282-0
Support	+49 911 97282-14
Engineering	+49 911 97282-13
E-Mail	iba@iba-ag.com
Web	www.iba-ag.com

Issue	Date	Revision	Author	Version HW/FW
1.0	09-2024	First issue	CV, st	1.0

Certification

The product is certified according to the European standards and directives. This product meets the general safety and health requirements.

Other international and national standards were observed.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Contents

1 About this documentation

This documentation describes the design, application and operation of the device *ibaFOB-R*.

1.1 Target group

This documentation is aimed at qualified professionals who are familiar with handling electrical and electronic modules as well as communication and measurement technology. A person is regarded as professional if he/she is capable of assessing safety and recognizing possible consequences and risks on the basis of his/her specialist training, knowledge and experience and knowledge of the standard regulations.

1.2 Notations

In this manual, the following notations are used:

Action	Notation
Menu command	Menu *Logic diagram*
Calling the menu command	*Step 1 – Step 2 – Step 3 – Step x* Example: Select the menu *Logic diagram – Add – New function block*.
Keys	<Key name> Example: <Alt>; <F1>
Press the keys simultaneously	<Key name> + <Key name> Example: <Alt> + <Ctrl>
Buttons	<Key name> Example: <OK>; <Cancel>
Filenames, paths	`Filename`, `Path` Example: `Test.docx`

1.3 Used symbols

If safety instructions or other notes are used in this manual, they mean:

Danger!

The non-observance of this safety information may result in an imminent risk of death or severe injury:

- Observe the specified measures.

Warning!

The non-observance of this safety information may result in a potential risk of death or severe injury!

- Observe the specified measures.

Caution!

The non-observance of this safety information may result in a potential risk of injury or material damage!

- Observe the specified measures

Note

A note specifies special requirements or actions to be observed.

Tip

Tip or example as a helpful note or insider tip to make the work a little bit easier.

Other documentation

Reference to additional documentation or further reading.

2 About ibaFOB-R

The *ibaFOB-R* board is a PCI Express (PCIe) member of the iba family of fiber optic boards. The board supports both low profile and standard height PCIe slots.

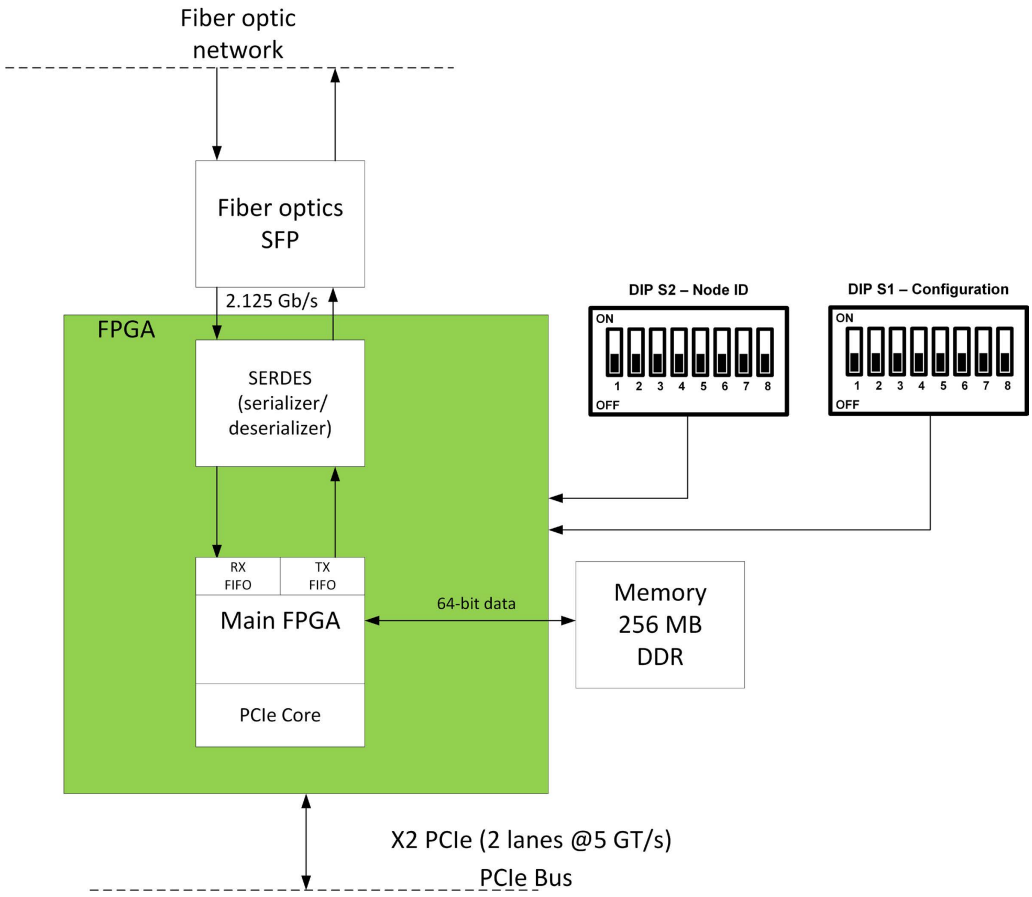
The *ibaFOB* board is network compatible with other Reflective Memory products working on 2.125 Gbaud.

Two or more *ibaFOB* boards, along with other members of the Reflective Memory family, can be integrated into a network using standard fiber-optic cables. Each board in the network is referred to as a “node”.

Reflective Memory allows computers, workstations, PLCs and other embedded controllers with different architectures and dissimilar operating systems to share data in real time. *ibaFOB-R* is fast, flexible and easy to operate.

Data is transferred by writing to local RAM memory, which appears to reside globally in all boards on the network.

On-board circuitry automatically performs the data transfer to all other nodes with little or no involvement of any host processor. A block diagram of the *ibaFOB-R* board is shown in the following figure.



2.1 Features

The features of *ibaFOB-R* board include:

- High speed, easy to use fiber-optic network (2.125 Gbaud serially)
- PCI Express interface (up to 2 active lanes over a 4x connector, speed up to Gen2)
- No host processor involvement in the operation of the network
- Up to 256 nodes
- Up to 500 m on 50/125 µm multimode fiber, 300 m on 62.5/125 µm multimode fiber
- Dynamic packet size, 4 to 64 bytes of payload data per packet
- Fiber network transfer rate 40 MB/s to 162 MB/s
- 256 MB Reflective Memory
- Independent Direct Memory Access (DMA) channel
- Four general purpose network interrupts; each with 32 bits of data
- Selectable PCI PIO window size (2 MB, 16 MB, 64 MB, 256 MB)
- RoHS compliant

2.2 PCI Express Compliance

The *ibaFOB-R* board is designed to interface with any suitable PCIe compliant motherboard using a PCIe 4x slot connector (or larger). The *ibaFOB-R* board complies with requirements of the PCI Express Specification, Revision 2.1.

2.3 Vendor and Device identification

The PCI Configuration register reserved for the Vendor ID has the value of 0x167F, which designates iba AG.

The PCI Configuration register reserved for the Device ID has the value of 0x5565. The value indicates the iba AG board type for this board and also indicates the Reflective Memory family type.

3 Safety instructions

Observe the following safety instructions for *ibaFOB-R*.

3.1 Intended use

The device is an electrical apparatus. It must only be used for the following applications:

- Automation of industrial plants
- Measurement data acquisition and analysis
- Applications of iba software products (*ibaPDA*)

The use of the *ibaFOB-R* board in third-party systems is only possible after consultation with iba AG.

3.2 Special safety instructions

Danger from electric shock!

Disconnect the power supply from the computer before opening the device to avoid an electric shock!

Do not install or remove the card while the power supply is switched on.

Caution!

Electrostatic discharges can damage the board! To avoid electrostatic ESD damage, discharge your body electrically before touching the electronic board.

You can discharge your body by touching a conductive, grounded object immediately before working with the board (e.g. metal cabinet components, socket protective conductor contact).

4 Scope of delivery

After having unpacked the delivery, please check it for completeness and possible damage.

The scope of delivery comprises:

- *ibaFOB-R* board with standard bracket installed
- A multimode SFP module installed
- Low profile bracket to replace the standard bracket to install the board in low profile PCIe slots

For more accessories not included in the delivery (such as FO cables), please see www.iba-ag.com.

5 System requirements

Observe the following requirements for using the *ibaFOB-R* board.

Hardware

Windows computer with the following minimum configuration:

- Pentium IV/3 GHz
- At least one free PCIe 2.0-x4 compatible slot
- 4 GByte RAM
- Free disk space > 10 GByte

For more information about iba industrial computer, please see www.iba-ag.com.

Software

- *ibaPDA* version 8.8 or higher

6 Installing and removing the board

Observe the following warnings when working with the board.

Danger from electric shock!

Disconnect the power supply from the computer before opening the device to avoid an electric shock!

Do not install or remove the card while the power supply is switched on.

Caution!

Electrostatic discharges can damage the board! To avoid electrostatic ESD damage, discharge your body electrically before touching the electronic board.

You can discharge your body by touching a conductive, grounded object immediately before working with the board (e.g. metal cabinet components, socket protective conductor contact).

6.1 Installing the board

1. Shut down the PC.
2. Unplug the mains power line and open the PC so you can reach the PCIe slots.
3. Take the board carefully out of the package. Use a grounding cable or discharge any electrostatic charge before taking the board.
4. Grab the board at the front plate and the rear upper corner. Do not touch the contacts. Set the S1 and S2 switches as explained in chapter ↗ *Configuration*, page 18.
5. The *ibaFOB-R* is a low profile form factor board.

   The board is shipped assembled with a full-height bracket. A low profile bracket is included in the package. If your computer requires a low profile board, replace the full-height bracket on the board with the supplied low profile bracket.
6. Plug in the board carefully into a free PCIe slot and fix the board to the housing of the PC.
7. Close the PC.
8. Plug in the power line and start the PC.

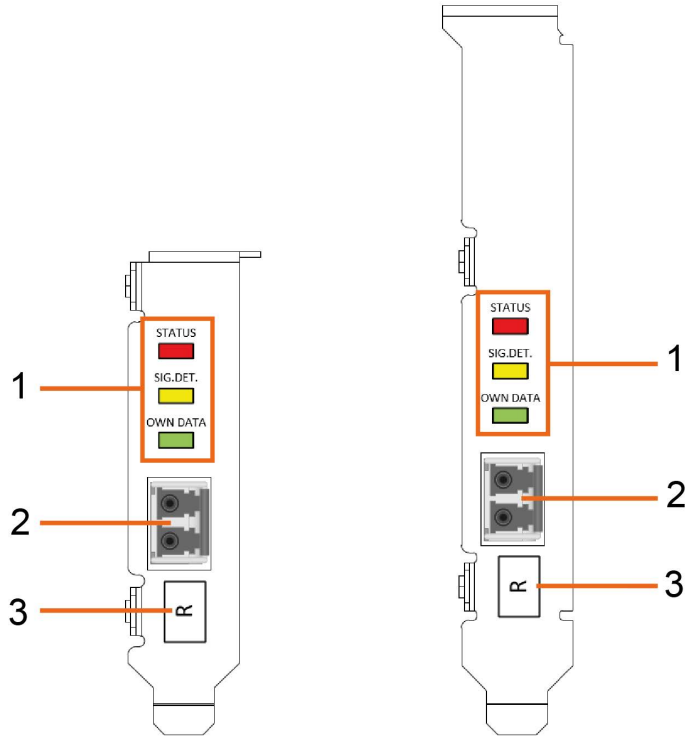
6.2 Removing the board

1. Shut down the PC.
2. Unplug the mains power line and open the PC so you can reach the PCIe slots.
3. Disconnect all external connections from the board.
4. Release the fixing screw.
5. Unplug the board carefully out of the slot. Store the board in an appropriate container.

7 Description

Here you will find views and descriptions of the *ibaFOB-R* board.

7.1 Front view



Left: *ibaFOB-R* board with low profile bracket, right: *ibaFOB-R* board with standard bracket

1 Operating status indicators

2 Fiber optic connection (SFP)

3 Identifier for boards of the ibaFOB family

The identifier (3) is used to distinguish the individual ibaFOB board types. The following identifier stands for the following board types:

D ibaFOB-D and ibaFOB-Dexp

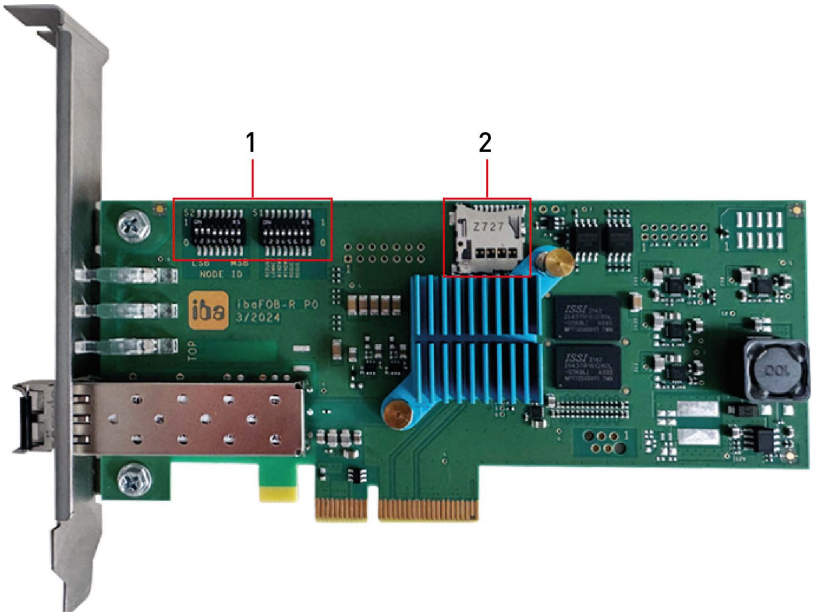
TDC ibaFOB-TDC and ibaFOB-TDCexp

SD ibaFOB-SD and ibaFOB-SDexp

PC ibaFOB-PlusControl

R ibaFOB-R

7.2 Top view



1 DIP switches, see also chapter ↗ *Configuration*, page 18

2 SD slot, for service purposes only

7.3 Display elements

The operating status of the device is shown by colored status LEDs.

LED	Color	Description
Status	Red/off	User defined status indicator. Controlled by the host. Can be set to blinking by *ibaPDA* – I/O Manager
	Blue	The host system has disabled the board on the PCIe bus. (The board is in PCI Power Management state D3 or kept in Reset.)
Signal Detect	Yellow	Valid optical signal detected on the optical network connection
	Blue	Invalid optical signal detected on the optical network connection
	off	No optical signal detected on the optical network connection
Own Data	Green	Indicates when own transmitted packets are received back

The Status LED's power up default state is ON.

The Status LED is a user defined board indicator and can be toggled ON or OFF by writing to Bit 31 of the Control and Status register.

The Signal Detect LED turns ON if the receiver detects light. It can be used as a simple method of checking that the optical network is properly connected to the receiver.

The Own Data LED is turned ON when the board has detected its own data returning over the network. The LED can be turned OFF by clearing Bit 0 of the Control and Status register.

7.4 Fiber optic connections

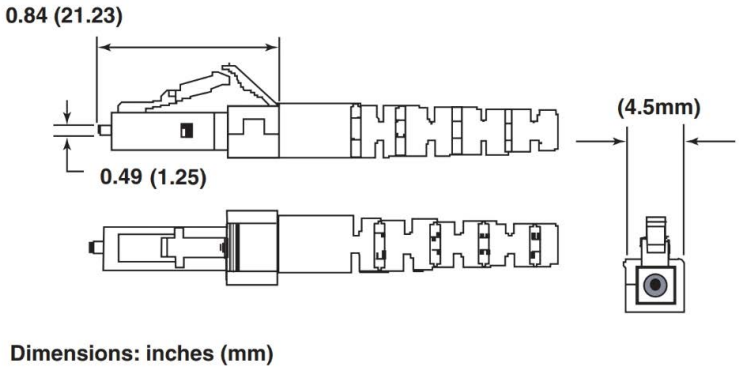
In the fiber optic Small Form-factor Pluggable (SFP) interface of the *ibaFOB-R* board, a single-mode SFP or multimode SFP can be installed.

The following table below gives an overview of the cable specification for both singlemode and multimode fibers.

Specification	Singlemode	Multimode
Core Diameter	8.3 ±1.0 µm	50/62.5 ±3 µm
Cladding Diameter	125 ±2 µm	125 ±2 µm
Jacket Outer Diameter	3.0 mm ±0.1 mm	3.0 mm ±0.1 mm
Attenuation	0.8 dB/km (max) at 1310 nm	4.0 dB/km (max) at 850 nm
Bandwidth	N/A	160 to 300 MHz*km (min) at 850 nm
UL	type OFNR, CSA type OFN FT4	type OFNR, CSA type OFN FT4

The *ibaFOB-R* board is delivered with a multimode SFP module installed, using LC type fiber optic connectors.

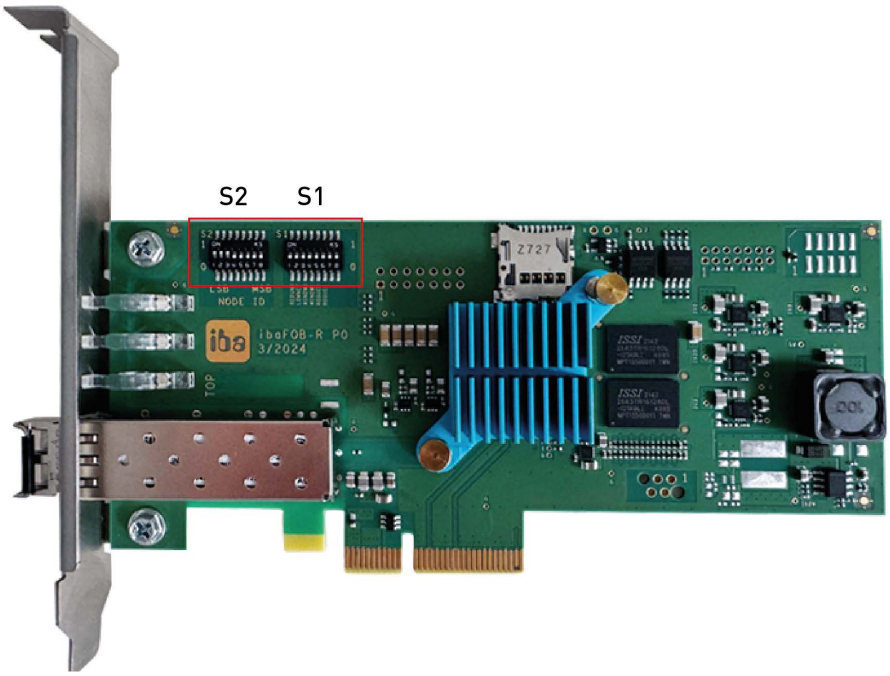
LC type fiber optic connectors:



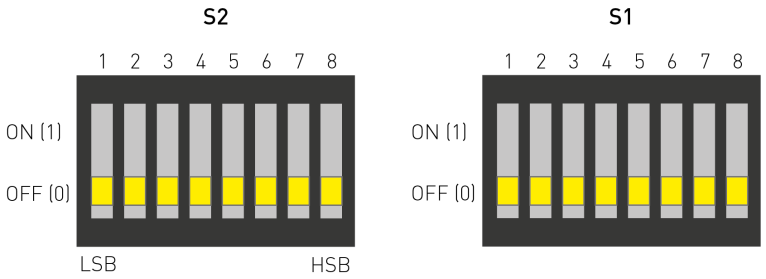
8 Configuration

Prior to installing the board, a number of settings must be configured using 2 DIP (dual in-line package) switches S1 and S2 on the *ibaFOB-R* board.

The following illustration shows the arrangement of switches S1 and S2.



Factory defaults of the DIP switches:



8.1 Switch S1 configuration

Prior to installing the *ibaFOB-R* board into the host system, switch S1 must be configured for the appropriate mode of operation. Switch S1 controls six functions on the board.

Settings on Switch S1 should only be changed while power is off.

Tip

In most cases there is no need to do the S1 configuration. It can therefore remain in the default state with all switches in the OFF state.

- S1 position 1: selects the redundant (ON) or non-redundant (OFF) network transfer mode.
- S1 position 2 reduces the transmission rate of the board onto the network in order to avoid congestion for other network participants (ON). Full transmission bandwidth is available when OFF.
- S1 positions 3 and 4: select the PCI window size for PIO memory accesses. The default (when both switch positions 3 and 4 are OFF) is to use the full installed memory size. The reduced memory window size choices are 64 MB, 16 MB or 2 MB.
- S1 position 5 enables (ON position) or disables the Rogue Master 0 function.
- S1 position 6 enables (ON position) or disables the Rogue Master 1 function.
- S1 position 7: currently reserved (should be left in the OFF position).
- S1 position 8: currently reserved (should be left in the OFF position).

The tables below gives an overview of the S1 settings.

Switch S1 configuration settings

Position 1	OFF: non-redundant mode ON: redundant mode	Position 2	OFF: full transmission bandwidth ON: reduced transmission bandwidth
Position 5	OFF: disables Rogue Master 0 ON: enables Rogue Master 0	Position 6	OFF: disables Rogue Master 1 ON: enables Rogue Master 1
Position 3 and 4 : see table below		**Factory Default:** Positions 1-8 OFF	

Switch S1 PCI Window configuration

PCI Window Size	S1 Position 3	S1 Position 4
256 MB (default)	OFF	OFF
64 MB	ON	OFF
16 MB	OFF	ON
2 MB	ON	ON

8.2 Switch S2 configuration

Prior to installing the *ibaFOB-R* in a host system, the desired node ID must be set using switch S2. Each node in the network must have a unique node ID.

Switch S2 corresponds to 8 node ID select signal lines. The 8 node ID select lines permit any binary node ID from 0x00 to 0xFF (255 decimal).

Switch S2 position 1 (on the left!) corresponds to the least significant node ID line and switch S2 position 8 (on the right!) corresponds to the most significant node ID line.

Placing switch S2 in the OFF position sets the binary node ID line low (0), while placing switch S2 in the ON position sets the binary node ID line high (1).

The following table provides examples of possible node IDs.

S2 Pos. 1	S2 Pos. 2	S2 Pos. 3	S2 Pos. 4	S2 Pos. 5	S2 Pos. 6	S2 Pos. 7	S2 Pos. 8	Node ID Hex (Dec.)
ON	ON	ON	ON	ON	ON	ON	ON	0xFF (255)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	0x80 (128)
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	0x40 (64)
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	0x20 (32)
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	0x10 (16)
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	0x8 (8)
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	0x4 (4)
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	0x2 (2)
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0x1 (1)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0x0 (0)
Factory default: positions 1-8 OFF								

8.2.1 Important remarks before installation

Observe the following notes when configuring switches S1 and S2:

Note

Each Reflective Memory module on your Reflective Memory network must have a unique node ID to identify itself. So before setting the node ID by switch S2, check the node ID of all other participants on the network. There is no inherent detection of duplicate nodes on a network!

Note

ALL nodes on the ring MUST be configured for the SAME transfer mode, either redundant or non-redundant transfer mode. A mismatch of this setting will result in certain packets being removed from the ring, and that data will be lost.

Note

No more than one node on the ring should be configured with Rogue Master 0 enabled. Certain packets will be removed from the ring when two or more nodes are configured with Rogue Master 0 enabled, and that data will be lost.

Note

No more than one node on the ring should be configured with Rogue Master 1 enabled. Certain packets will be removed from the ring when two or more nodes are configured with Rogue Master 1 enabled, and that data will be lost.

9 Configuration in ibaPDA

This manual describes all the features of the *ibaFOB-R* board when used in the *ibaPDA* system, including additional diagnostics and troubleshooting information.

Other documentation

For configuration in *ibaPDA*, please refer to manual *ibaPDA-Interface-Reflective-Memory*.

For data acquisition via Reflective Memory with *ibaPDA*, the interface license *ibaPDA-Interface-Reflective-Memory* (31.001220) has to be purchased separately (as in the past with ABACO and former Reflective Memory boards).

10 System integration

Note

This chapter is intended for system integrators who want to use the *ibaFOB-R* board in their own automation or embedded system.

For users of the *ibaFOB-R* board together with *ibaPDA*, this detailed information is less relevant.

The following sections describe the functionality of the *ibaFOB-R* board. A description of the major sub-circuits and their operation is included.

This section will also occasionally mention Control and Status registers related to operations. To see a detailed description of these Control and Status registers please refer to chapter ↗ *Programming requirements*, page 26.

10.1 Basic functionality and operation

Each node in the Reflective Memory network is interconnected using fiber-optic cables in a daisy chain loop. The transmitter of the first board must be connected to the receiver of the second board. The transmitter of the second board is connected to the receiver of the third, and so on, until the loop is completed back at the receiver of the first board.

Alternatively, any node can be connected to the ring network using one or more Reflective Memory hubs.

It is important that the ring network is complete (i.e., every receiver and transmitter must be connected). Each node must have a unique node ID, which is set using switch S2 (i.e. no two nodes should have the same node ID). The order of the node IDs is unimportant.

A transfer of data over the network is initiated by a write from the host system to the onboard RAM memory. The write can be as simple as a PIO target write, or it can be due to a DMA cycle by the resident DMA engine.

While the write to the RAM is occurring, circuitry on the *ibaFOB-R* board automatically writes the data and other pertinent information into the transmit FIFO.

From the transmit FIFO, the transmit circuit retrieves the data and puts it into a variable length packet of 4 to 64 bytes that is transmitted over the fiber-optic interface to the receiver of the next board. The receiver then checks the packet for errors. When the error free data is received, the receive circuit stores the data in the board's receive FIFO. From the receive FIFO, another circuit writes the data into the local onboard RAM at the same relative location in memory as the originating node.

This circuit also simultaneously routes the data into the board's own transmit FIFO. From there, the process is repeated until the data returns to the receiver of the originating node. At the originating node, the data packet is removed from the network.

10.2 ibaFOB-R hardware registers

Users who want to go beyond the standard read write operations, must understand and manipulate bits within three register sets. The three register sets are:

- PCI Configuration Registers, see ↗ *PCI Configuration Registers*, page 27
- Local Configuration Registers, see ↗ *Local Configuration Registers*, page 35
- RFM Control and Status Registers, see ↗ *RFM Control and Status Registers*, page 38

PCI Configuration Registers
This set of registers is predefined by the PCI Local Bus Specification and is standard for all PCI and PCI Express devices. This register set contains the Vendor ID, Device ID, Subsystem Vendor ID and Base Address registers. The PCI Configuration Registers are first initialized and then modified as needed by the PCI bus system BIOS. The register set is rarely altered by the user, but the ability to read these registers, particularly the Base Address Registers, will be necessary to locate the other two sets of registers.

Local Configuration Registers
Base Address Register 0 contains the starting address for the Local Configuration Registers. Some Local Configuration Registers pertinent to the *ibaFOB-R*'s operation include the Interrupt Control and Status Register (INTCSR) and the DMA Control Registers.

RFM Control and Status Registers
The RFM Control and Status Registers implement the functions unique to the *ibaFOB-R* Reflective Memory board. These functions include RFM operation status, detailed control of the RFM sources for the PCI interrupt, and network interrupt access. These registers are accessed starting at the address contained in Base Address Register 2.

10.3 Reflective Memory RAM on ibaFOB-R

The *ibaFOB-R* board is available with 256 MB of onboard Reflective Memory RAM.

The RAM starts at the location specified in Base Address Register 3.

The offset address range is 0 to 0xFFFFFFF for 256 MB.

This address range can be limited by setting the S1 switch accordingly, see chapter ↗ *Switch S1 configuration*, page 18.

10.4 Interrupt generation

The *ibaFOB-R* board has a single interrupt output on the PCIe bus.

The interrupt can be generated as a legacy INTA# message level interrupt or as an MSI or MSI-X event interrupt when enabled by the system software.

One or more events on the *ibaFOB-R* board can cause the interrupt. The sources of the interrupt can be individually enabled and monitored through several registers. The interrupt circuitry of the *ibaFOB-R* board is arranged in two tiers.

The primary tier of interrupts is enabled and monitored by the Local Configuration Register's INTCSR at offset 0x68. The sources for the primary tier interrupts are:

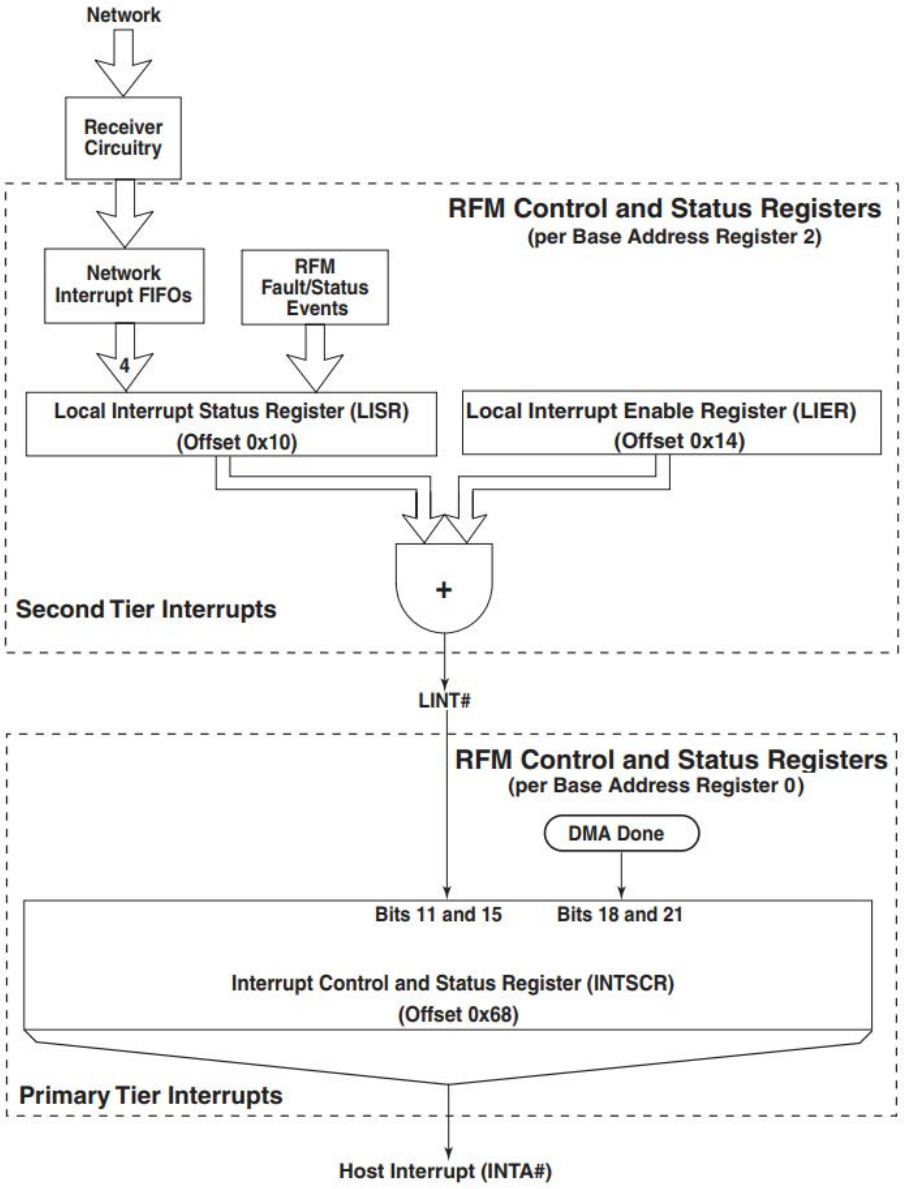
1. DMA Done
2. Local Interrupt Input

The primary tier interrupt source (1) can be used to report the end of a DMA transfer and it must be configured in the DMA registers. The other primary tier interrupt source (2) is the Local Interrupt Input.

All secondary tier interrupts are funneled through the Local Interrupt Input. Second tier interrupts include several operational status bits, faults, and network interrupts. The second tier interrupts are selected and monitored through the two RFM Control and Status Registers referred to as the Local Interrupt Status Register (LISR) and the Local Interrupt Enable Register (LIER).

For a detailed description of these two registers refer to chapter. ↗ *RFM Control and Status Registers*, page 38

A block diagram of the interrupt circuit is shown in the following figure.



10.5 Network interrupts

The *ibaFOB-R* board is capable of passing interrupt packets, as well as data packets, over the network. The network interrupt packets can be directed to a specific node or broadcast globally to all other nodes on the network. Each network interrupt packet contains the sender's node ID, the destination node ID, the interrupt type and 32 bits of user defined data.

The types of network interrupts include four general purpose interrupts and a reset node request interrupt. Node specific interrupts are sent by configuring three RFM Control and Status registers. Each receiving node evaluates the interrupt packets as they pass through. If a general purpose interrupt is directed to that node, then the sender's node ID is stored in the appropriate Sender ID FIFO (one of four). Each Sender ID FIFO is at least 127 locations deep. The accompanying data will be stored in a companion data FIFO.

If enabled through the LISR, LIER and INTCSR registers, any of the network interrupts can also generate a host PCI interrupt at each receiving node.

The reset node request interrupt is not stored in a FIFO like the four general purpose interrupts. Furthermore, it does not cause an immediate reset of the board. Instead, it sets a bit in the LISR register, which will result in a PCI interrupt if enabled. The actual board reset should be performed by the host system in an orderly fashion. However, the user application could use this network interrupt for any purpose.

10.6 Redundant Transfer mode

The *ibaFOB-R* board is capable of operating in a redundant transfer mode. The board is configured for redundant mode when switch S1 position 1 is in the ON position. In the redundant transfer mode, each generated packet transfers twice, regardless of the packet size. The receiving circuitry of each node on the network evaluates each of the redundant transfers. If no errors are detected in the first transfer, it is used to update the onboard memory and the second transfer is discarded. However, if the first transfer contains an error, the second transfer is used to update the onboard memory provided it has no transmission errors. If errors are detected in both transfers, the transfers will not be used and the data is completely removed from the network.

Redundant transfer mode reduces the chance that any data is dropped from the network. However, the redundant transfer mode also reduces the network data transfer rate. The single DWord (Double-word = 4 byte) transfer rate drops from the non-redundant rate of 43 MB/s to approximately 20 MB/s. The 16 DWord (64 byte) transfer rate drops from the non-redundant rate of 170 MB/s to the redundant rate of 85 MB/s.

10.7 Rogue Packet Removal Operation mode

A rogue packet is a packet that does not belong to any node on the network. Recalling the basic operation of Reflective Memory, one node originates a packet on the network in response to a memory write from the host. The packet is transferred around the network to all nodes until it returns to the originating node. It is a requirement that the originating node removes the packet from the network. If, however, the packet is erroneously altered as it passes through another node, or if the originating node begins to malfunction, then the originating node may fail to

recognize the packet as its own and will not remove it from the network. In this case, the packet will continue to traverse the network as a “rogue packet.”

Rogue packets are extremely rare. A rogue packet could be created when turning a node’s power on or off while connected to an optical Hub. It could also occur when connecting or disconnecting fiber cables. A rogue packet might be created if any node in the network overflows a network FIFO. Their existence could indicate a malfunctioning board due to true component failure, or due to operation in an overly harsh environment. Normally, the solution is to isolate and replace the malfunctioning board and/or improve the environment. However, some users prefer to tolerate sporadic rogue packets rather than halt the system for maintenance provided the rogue packets are removed from the network.

To provide tolerance for rogue packet faults, the *ibaFOB-R* board contains circuitry that allows it to operate as one of two Rogue Masters. A rogue master marks each packet as it passes through from another node. If the same packet returns to the rogue master a second time, the Rogue Master recognizes that it is a rogue packet and removes it from the network (after the rogue packet has affected every node). When a rogue packet is detected, a rogue packet fault flag is set in the LISR. The assertion of the rogue packet fault bit may optionally assert a PCI interrupt to inform the host that the condition exists. Two rogue masters, Rogue Master 0 and Rogue Master 1, are provided to cross check each other. Rogue Master 0 is enabled by placing switch S1 position 5 in the ON position. Rogue Master 1 is enabled by placing switch S1 position 6 in the ON position. Just as two boards in a network should not have the same node ID, two boards in the same network should not be set as the same Rogue Master. Otherwise, one of the two will erroneously remove packets marked by the other.

10.8 Programming requirements

Basic target write and read operations of the *ibaFOB-R*- board require little or no software.

The board powers up in a functional mode. The user will need to access the PCI Configuration registers (Base Address Register 0, 2 and 3) to learn where the system BIOS has located the other register sets and the Reflective Memory.

The location of the register sets and the Reflective Memory varies from system to system and can even vary from slot to slot within a system.

For operations beyond the basic setup, such as enabling or disabling interrupts or performing DMA cycles, the user must know the specific bit assignments of the registers within the three register sets. That information is provided in this chapter.

The three register sets are:

- PCI Configuration Registers
- Local Configuration Registers
- RFM Control and Status Registers

10.8.1 PCI Configuration Registers

The PCI Configuration registers are located in 256 bytes of the PCI Configuration Space, which follows a template defined by the PCI Specification.

Although the PCI Configuration registers are accessible at all times, they are rarely altered by the user application. In most cases these are configured by system software.

PCI Configuration Registers

Address (Hex)	31..24	23..16	15..8	7..0
00	Device ID		Vendor ID	
04	Status Register		Command Register	
08	Class Code			Revision ID
0C	BIST*	Header Type	Latency Timer*	Cache Line Size*
10	Base Address Register 0			
14	Base Address Register 1*			
18	Base Address Register 2			
1C	Base Address Register 3			
20	Base Address Register 4*			
24	Base Address Register 5*			
28	Cardbus CIS Pointer*			
2C	Subsystem ID		Subsystem Vendor ID	
30	Expansion ROM Base Address*			
34	Reserved*			Capabilities Pointer
38	Reserved*			
3C	Max_Lat*	Min_Gnt*	Interrupt Pin	Interrupt Line
40..47	Power Management Capability Structure			
48..4F	MSI Capability Structure			
50..5F	Reserved*			
60..9B	PCIe Capability Structure			
9C..A7	MSI-X Capability Structure			
A8..FF	Reserved*			
Cells marked with * indicate reserved or non-applicable registers for *ibaFOB-R* (value undefined after reset)				

PCI Configuration ID Registers (Offset 0x00)

Bit	Description	Read	Write	Value after PCI Reset
15:0	**Vendor ID** Identifies manufacturer of device	Yes	No	0x167F **= iba AG**
31:16	**Device ID** Identifies particular device	Yes	No	0x5565

PCI Command Register (Offset 0x04)

Bit	Description	Read	Write	Value after PCI Reset *
0	**I/O Space** Writing a one (1) allows the device to respond to I/O Space accesses. Writing a zero (0) disables the device from responding to I/O Space accesses	Yes	Yes	0
1	**Memory Space** Writing a one (1) allows device to respond to Memory Space accesses. Writing a zero (0) disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Bus Master Enable** Writing a one (1) allows the device to behave as a bus master (required for DMA and for sending MSI/MSI-X interrupts) Writing a zero (0) disables the device from generating bus master accesses.	Yes	Yes	0
3	**Special Cycle Enable** Not applicable to PCI Express	Yes	No	0
4	**Memory Write and Invalidate** Not applicable to PCI Express	Yes	No	0
5	**VGA Palette Snoop** Not applicable to PCI Express	Yes	No	0
6	**Parity Error Response** Report PCIe poisoned completion TLP when enabled (1) in the PCI Status Register	Yes	Yes	0
7	**Wait Cycle Control** Not applicable to PCI Express	Yes	No	0

Bit	Description	Read	Write	Value after PCI Reset *
8	**SERR# Enable** Report PCIe Fatal and Non-fatal Errors when enabled (1)	Yes	Yes	0
9	**Fast Back-to-Back Transaction Enable** Not applicable to PCI Express	Yes	No	0
10	**Interrupt Disable** When set (1) disables the *ibaFOB-R* from sending legacy interrupt messages (INTA#). This bit has no influence on MSI/MSI-X interrupts. When cleared (0) INTA# interrupt messages are generated normally.	Yes	Yes	0
15:11	**Reserved**	Yes	No	0
*Note: This register will likely be altered by system software during the system boot process (e.g. 0x0106).				

PCI Status Register (Offset 0x06)

Bit	Description	Read	Write	Value after PCI Reset
2:0	**Reserved**	Yes	No	0x0
3	**Interrupt Status** Set by the *ibaFOB-R* board when the function would normally assert an interrupt pin, regardless of interrupt disable bit state.	Yes	No	0
4	**New Capabilities Functions Support** Hardwired to a one (1). The *ibaFOB-R* implements a capabilities list.	Yes	No	1
5	**66 MHz Capable** Not applicable to PCI Express	Yes	No	0
6	**Reserved**	Yes	No	0
7	**Fast Back-to-Back Capable** Not applicable to PCI Express	Yes	No	0
8	**Master Data Parity Error** When set (1), indicates the *ibaFOB-R* board has detected a poisoned completion, but only if the Parity Error Response bit is set in the Command Register.	Yes	Yes/Clr	0

Bit	Description	Read	Write	Value after PCI Reset
10:9	**DEVSEL# Timing** Not applicable to PCI Express	Yes	No	0
11	**Signaled Target Abort** When set (1), indicates the *ibaFOB-R* board has signaled a Completer Abort. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
12	**Received Target Abort** When set (1), indicates the *ibaFOB-R* board has received a Completer Abort response. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
13	**Received Master Abort** When set (1), indicates the *ibaFOB-R* board has received an Unsupported Request response Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
14	**Signaled Signal System Error** When set (1), indicates the *ibaFOB-R* board has sent an ERR_FATAL or ERR_NONFATAL message if the SERR# Enable is set in the Command Register. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
15	**Detected Parity Error** When set (1), indicates the *ibaFOB-R* board has detected a poisoned TLP, regardless of the state of the Parity Error Response bit in the Command Register. Writing a one (1) clears this bit to zero (0)	Yes	Yes/Clr	

PCI Revision ID Register (Offset 0x08)

Bit	Description	Read	Write	Value after PCI Reset
7:0	**Revision ID** Revision number of the board	Yes	No	Current Rev#

PCI Class Code Register (Offset 0x09)

Bit	Description	Read	Write	Value after PCI Reset
7:0	**Register Level Programming Interface.** None defined.	Yes	No	0x0
15:8	**Subclass Code**	Yes	No	0x80
23:16	**Base Class Code**	Yes	No	0x02
Base Class Code of 0x02 equals *Network Controller*. Subclass Code of 0x80 equals *Other Network Controller*.				

PCI Header Type Register (Offset 0x0E)

Bit	Description	Read	Write	Value after PCI Reset
6:0	**Configuration Layout Type** Zero (0) indicates an Endpoint device.	Yes	No	0x0
7	**Header Type** Zero (0) indicates a single function device.	Yes	No	0x0

PCI Base Address Register 0 contains the starting address for memory mapped access to the Local Configuration Registers. The value in this register is configured by the system BIOS.

PCI Base Address Register 0 (Offset 0x10) [Local Configuration Registers]

Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator** 0 indicates the register maps into Memory Space.	Yes	No	0
2:1	**Register Location** 00 - Locate anywhere in 32-bit Memory Address Space	Yes	No	00
3	**Prefetchable Indicator** 0 indicates non-prefetchable	Yes	No	0
8:4	**Memory Base Address** Hardcoded to 0x0 to indicate a size of 512 bytes	Yes	No	0x0
31:9	**Memory Base Address** Memory Base Address for access to Local Configuration registers	Yes	Yes	0x0
*Note: This register will be altered by the system BIOS during the system boot process.				

PCI Base Address Register 1 is not used in the *ibaFOB-R* board.

PCI Base Address Register 2 contains the starting address for memory mapped access to the RFM Control and Status Registers. The value in this register is configured by the system BIOS.

PCI Base Address Register 2 (Offset 0x18) [RFM Control and Status]

Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator** 0 indicates the register maps into Memory Space.	Yes	No	0
2:1	**Register Location** 00 - Locate anywhere in 32-bit Memory Address Space	Yes	No	00
3	**Prefetchable Indicator** 0 indicates non-prefetchable	Yes	No	0
6:4	**Memory Base Address** Hardcoded to 0x0 to indicate a size of 128 bytes	Yes	No	0x0
31:7	**Memory Base Address** Memory Base Address for access to RFM Control and Status registers	Yes	Yes	0x0
*Note: This register will be altered by the system BIOS during the system boot process.				

PCI Base Address Register 3 contains the starting address for memory mapped access to the Reflective Memory RAM. The value in this register is configured by the system BIOS. It depends on the settings of S1 switch positions 3 and 4. The address offset range is:

- 0x0 to 0x01FFFFF for the 2 MB window setting,
- 0x0 to 0x0FFFFFF for the 16 MB window setting,
- 0x0 to 0x3FFFFFF for the 64 MB window setting,
- 0x0 to 0xFFFFFFF for 256 MB if windowing is deactivated by S1

PCI Base Address Register 3 (Offset 0x1C) [Reflective Memory RAM]

Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator** 0 indicates the register maps into Memory Space.	Yes	No	0
2:1	**Register Location** 00 - Locate anywhere in 32-bit Memory Address Space	Yes	No	00

Bit	Description	Read	Write	*Value after PCI Reset
3	**Prefetchable Indicator** 0 indicates non-prefetchable	Yes	No	0
31:4	**Memory Base Address**. Memory Base Address for access to Reflective Memory RAM (size depending on windowing as explained above)	Yes	Yes	0x0
*Note: This register will be altered by the system BIOS during the system boot process.				

PCI Base Address Register 4 and 5 are not used in the *ibaFOB-R* board.

PCI Subsystem Vendor ID Register (Offset 0x2C)

Bit	Description	Read	Write	Value after PCI Reset
15:0	Subsystem Vendor ID	Yes	No	0x167F **= iba AG**

PCI Subsystem ID Register (Offset 0x2E)

Bit	Description	Read	Write	Value after PCI Reset
15:0	Subsystem ID	Yes	No	0x5565

PCI Capabilities Pointer Register (Offset 0x34)

Bit	Description	Read	Write	Value after PCI Reset
7:0	**Capabilities Pointer** Offset into PCI Configuration Space for the location of the first item in the PCI Capabilities Linked List.	Yes	No	0x40

PCI Interrupt Line (Offset 0x3C)

Bit	Description	Read	Write	*Value after PCI Reset
7:0	**Interrupt Line Routing Value** Value used by the operating system to indicate to which input of the system interrupt controller the (virtual) interrupt line of the device is connected to.	Yes	Yes	0x0
*Note: This register will be altered by the system BIOS during the system boot process.				

PCI Interrupt Pin (Offset 0x3D)

Bit	Description	Read	Write	Value after PCI Reset
7:0	**Interrupt Pin Register** Indicates which legacy interrupt pin the device uses. 1 = INTA# (*ibaFOB-R* only uses INTA# or message based MSI(-X) interrupts)	Yes	No	0x1

The *ibaFOB-R* board supports the following 4 standardized PCI Capability structures.

In general, these registers are managed by system software.

Capability structures

PCI Configuration space address	Capability ID	Description
0x40…0x47	0x01	The Power Management Capability Structure
0x48…0x4F	0x05	The MSI (Message Signaled Interrupt) Capability Structure
0x60…0x9B	0x10	The PCI Express Capability Structure
0x9C…0xA7	0x11	The MSI-X (extended MSI) Capability Structure

Tip

To find more detailed information about the various capability structures in PCI devices, you can refer to the PCI Local Bus Specification, which is maintained by the PCI-SIG (PCI Special Interest Group). The PCI Local Bus Specification outlines the standards and protocols for PCI devices, including the structure and usage of capability structures.

10.8.2 Local Configuration Registers

The Local Configuration Registers are accessible at the address specified by the value in Base Address Register 0. The offsets are specified below.

Local Configuration and DMA Control Registers

Offset from Base Address	Register Name	Writable
0x00-0x67	**Reserved**	N/A
0x68	Interrupt Control and Status (INTCSR)	Yes
0x6C-0x83	**Reserved**	N/A
0x84	DMA PCI Address	Yes
0x88	DMA RFM Address	Yes
0x8C	DMA Transfer Size	Yes
0x90	DMA Direction	Yes
0x94-0xA7	**Reserved**	N/A
0xA8	DMA Control and Status (DMACSR)	Yes
0xAC-0xB3	**Reserved**	N/A
0xB4	DMA PCI Upper Address	Yes
0xB8-0xEF	**Reserved**	N/A
0xF0	RFM Window Mask	No
0xF4	RFM Window Base Address	Yes
0xF8-0x1FF	**Reserved**	N/A

Interrupt Control and Status Register [BAR0.0x68]
Note: only relevant bits are described, other register bits are reserved (write zero to them)

Bit	Description	Read	Write	Value after PCI Reset
8	**PCI Interrupt Enable** Functions as global interrupt enable. Bit must be set to enable PCI interrupts.	Yes	Yes	1
11	**Local Interrupt Enable** Enables the local interrupt sources (RFM interrupts) to assert a PCI interrupt.	Yes	Yes	0
15	**Local Interrupt Active** When set (1) indicates the Local interrupt is active.	Yes	No	0

Bit	Description	Read	Write	Value after PCI Reset
18	**DMA Interrupt Enable** Enables the DMA interrupt to assert a PCI interrupt. Writing a zero (0) disables the DMA interrupt and it also clears the interrupt.	Yes	Yes	0
21	**DMA Interrupt Active** When set (1) indicates the DMA interrupt is active (DMA transfer has finished).	Yes	No	0

DMA PCI Address Register [BAR0.0x84]

Bit	Description	Read	Write	Value after PCI Reset
31:0	**DMA PCI Address Register** Indicates from where in PCI Memory space DMA transfers (read or write) start. The address can be aligned to any byte boundary. Note: Register BAR0.0xB4 must be set to zero for 32 bit PCI addresses.	Yes	Yes	0

DMA RFM Address Register [BAR0.0x88]

Bit	Description	Read	Write	Value after PCI Reset
27:0	**DMA RFM Address Register** Indicates from where in Reflective Memory space DMA transfers (read or write) start. The address can be aligned to any byte boundary.	Yes	Yes	0
31:28	**Reserved**	Yes	No	0

DMA Transfer Size Register [BAR0.0x8C]

Bit	Description	Read	Write	Value after PCI Reset
22:0	**DMA Transfer Size** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0
31:23	**Reserved**	Yes	No	0

DMA Direction Register [BAR0.0x90]

Bit	Description	Read	Write	Value after PCI Reset
2:0	**Reserved**	Yes	No	0
3	**DMA Direction of Transfer** 1 indicates transfer from the RFM to the host (PCI bus). 0 indicates transfer from the host (PCI bus) to the RFM.	Yes	Yes	0
31:4	**Reserved**	Yes	No	0

DMA Control & Status Register [BAR0.0xA8]

Bit	Description	Read	Write	Value after PCI Reset
0	**DMA Enable** Writing a one (1) enables channel to transfer data. Writing a zero (0) disables the channel from starting a DMA transfer.	Yes	Yes	0
1	**DMA Start** Writing a one (1) starts transferring data if the channel is enabled.	No	Yes Set	0
2	**Reserved**	No	No	0
3	**DMA Clear Interrupt** Writing a one (1) clears the DMA interrupt.	No	Yes Clr	0
4	**DMA Channel Idle** 0 indicates the DMA transfer is in progress. 1 indicates the DMA engine is ready for a new request.	Yes	No	1
31:5	**Reserved**	Yes	No	0

DMA PCI Upper Address Register [BAR0.0xB4]

Bit	Description	Read	Write	Value after PCI Reset
31:0	**DMA PCI Upper Address Register** The upper 32 bits of the 64 bit DMA PCI address must be specified here.	Yes	Yes	0

RFM Window Mask [BAR0.0xF0]

Bit	Description	Read	Write	Value after PCI Reset
31:0	**RFM Window Mask** Internally used mask depending on the RFM access window size	Yes	No	0xFFE00000 (for 2 MB) 0xFF000000 (for 16 MB) 0xFC000000 (for 64 MB) 0xF0000000 (for 256 MB)

RFM Window Base Address [BAR0.0xF4]

Bit	Description	Read	Write	Value after PCI Reset
0	**RFM Window Enable** The RFM access window is always enabled (1)	Yes	No	1
20:1	**Reserved**	Yes	No	0
27:21	**RFM Window Base Address (specified in 2 MB units)** Position of the access window within the 256 MB RFM zone. Window can only be positioned on multiples of the access window size. This register can be used to reach the complete 256 MB RFM for cases where the access window is smaller than 256MB.	Yes	Yes Depending on access window size	0
31:28	**Reserved**	Yes	No	0

10.8.3 RFM Control and Status Registers

The RFM Control and Status Registers are accessible at the address specified by the value in Base Address Register 2. The offsets are specified below.

Memory Map of the Local Control and Status Registers

Offset from Base Address	Mnemonic	Description	Writable	Comments
0x0	BRV	Board Revision	No	BRV is 0x8C
0x1	BID	Board ID Register	No	BID is 0x65
0x3..2	BRB	Board Revision Build	No	BRB depends on RFM window size
0x4	NID	Node ID Register	No	Configured by 8 switches of S2
0x7..5	--	**Reserved**	--	
0xB..8	LCSR1	Local Control & Status Reg. 1	Yes	Some bits reserved. Some bits read-only

Offset from Base Address	Mnemonic	Description	Writable	Comments
0xF..C	--	**Reserved**	--	
0x13..10	LISR	Local Interrupt Status Reg.	Yes	Some bits reserved. Some bits read-only
0x17..14	LIER	Local Interrupt Enable Reg.	Yes	
0x1B..18	NTD	Network Target Data	Yes	32 data bits for network interrupt target
0x1C	NTN	Network Target Node	Yes	Target node ID for network interrupt
0x1D	NIC	Network Interrupt Command	Yes	Select Int type and initiate network interrupt
0x1F..1E	--	**Reserved**	--	
0x23..20	ISD1	Int. 1 Sender Data	No	FIFO data for network interrupt 1
0x24	SID1	Int. 1 Sender ID	Yes/Clr	FIFO sender ID / read advances / write clears
0x27..25	--	**Reserved**	--	
0x2B..28	ISD2	Int. 2 Sender Data	No	FIFO data for network interrupt 2
0x2C	SID2	Int. 2 Sender ID	Yes/Clr	FIFO sender ID / read advances / write clears
0x2F..2D	--	**Reserved**	--	
0x33..30	ISD3	Int. 3 Sender Data	No	FIFO data for network interrupt 3
0x34	SID3	Int. 3 Sender ID	Yes/Clr	FIFO sender ID / read advances / write clears
0x37..35	--	**Reserved**	--	
0x3B..38	ISD4	Int. 4 Sender Data	No	FIFO data for network interrupt 4
0x3C	SID4	Int. 4 Sender ID	Yes/Clr	FIFO sender ID / read advances / write clears
0x3F..3D	--	**Reserved**	--	
0x4F..40	MSIX0	MSI-X Vector 0	Yes	Managed by system software
0x5F..50	MSIX1	MSI-X Vector 1	Yes	Managed by system software

Offset from Base Address	Mnemonic	Description	Writable	Comments
0x63..60	MSIXPBA	MSI-X Pending Bit Array	No	Managed by system software
0x65..64	RXU	Link Load	No	Incoming Link Load (in 1/256 %)
0x67..66	TXU	Own TX Load	No	Outgoing Link Load (in 1/256 %)
0x6F..68	FTIMER	**iba internal use**	No	FPGA Timer
0x73..70	FSTAT	FPGA status	No	FPGA status information
0x77..74	FINT	**iba internal use**	Yes	FPGA interrupt control
0x7B—78	FLASHC	**iba internal use**	Yes	FW update – flash access control
0x7F—7C	FLASHD	**iba internal use**	Yes	FW update – flash data

10.8.3.1 Board Revision Register (BRV) [BAR2.0x00]

An 8-bit register used to represent revisions or model numbers.

The current code is 0x8C. This register is read-only.

10.8.3.2 Board ID Register (BID) [BAR2.0x01]

An 8-bit register which contains an 8-bit code unique to the *ibaFOB-R* type boards.

The code is 0x65. This register is read-only.

10.8.3.3 Board Revision Build Register (BRB) [BAR2.0x2]

A 16-bit register used to represent the build number for this specific revision.

The lower four bits indicate the RFM window access size currently configured.

1 = 2 MB memory window

2 = 16 MB memory window

3 = 64 MB memory window

5 = 256 MB memory window

This register is read-only.

10.8.3.4 Node ID Register (NID) [BAR2.0x4]

An 8-bit register containing the node ID of the board.

This register reflects the setting of the switch S2 and is read-only. Each board on a network must have a unique node ID.

10.8.3.5 Local Control and Status Register 1 (LCSR1) [BAR2.0x08]

A 32-bit register containing Reflective Memory control and status bits as described below.

Local Control and Status Register 1

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status LED	Transmitter Disable	Dark-on-Dark Enable	Loopback Enable	Reserved	Redundant Mode Enabled	Rogue Master 1 Enabled	Rogue Master 0 Enabled
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	Window 1 Size (S1-4)	Total Size Config 1	Total Size Config 0	Window 0 Size (S1-3)	Low Network Usage Mode (S1-2)	Offset 1	Offset 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Reserved							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
TX FIFO Empty	TX FIFO Almost Full	Latched RX FIFO Full	Latched RX FIFO Almost Full	Latched Sync Loss	RX Signal Detect	Latched Bad Data	Latched Own Data

10.8.3.5.1 Local Control and Status Register 1 Bit Definitions

Bit 31	**Status LED** – This bit controls the user defined red status LED. Setting this bit low (0) turns the LED OFF. Setting this bit high (1) turns the LED ON. The default state of this bit after reset is high (1) and the LED will be ON.
Bit 30	**Transmitter Disable** – Setting this bit high (1) will manually turn OFF the board's transmitter. The default state of this bit after reset is low (0) and the transmitter is enabled. When turning the board's transmitter back ON by setting this bit back to low (0), an unspecified amount of time must be allowed to provide for the turn-on time of the optics.
Bit 29	**Dark-on-Dark Enable** – When this bit is set high (1), the board's transmitter will be turned OFF if the board's receiver does not detect a signal or if the receiver detects invalid data patterns. The dark-on-dark feature is useful in hub configurations.
Bit 28	**Loopback Enable** – When this bit is set high (1), the fiber optic transmitter is disabled and the transmit signal is looped back to the receiver circuit internally. This allows basic functional testing without an external cable.

Bit 26	**Redundant Mode Enabled** – When this bit is set high (1), redundant mode of network transfers has been enabled. This bit is read-only. Redundant mode is enabled by setting switch S1 position 1 in the ON position.
Bit 25	**Rogue Master 1 Enabled** – When this bit is set high (1), the board is operating as Rogue Master 1. This bit is read-only. Rogue Master 1 operation is enabled by setting switch S1 position 6 in the ON position.
Bit 24	**Rogue Master 0 Enabled** – When this bit is set high (1), the board is operating as Rogue Master 0. This bit is read-only. Rogue Master 0 operation is enabled by setting switch S1 position 5 in the ON position.
Bit 23	Reserved – This bit is reserved.
Bits 22 and 19	**Window 1 and Window 0** – The PCI access window size is selected by setting S1 switch positions 3 and 4. Bit 19 (Window 0) is connected to S1 switch position 3 (‘1’ when ON, ‘0’ when OFF). Bit 22 (Window 1) is connected to S1 switch position 4 (‘1’ when ON, ‘0’ when OFF). The two bits are read-only. These two bits indicate the RFM PCI access window size as defined in the table *Switch S1 PCI Window configuration*, see chapter ↗ *Switch S1 configuration*, page 18.
Bits 21 and 20	**Config 1 and Config 0** – These two bits indicate the installed memory size. The two bits are read-only. Config 1 is set to 1, Config 0 to 0 indicating 256 MB of installed memory.
Bit 18	**Low network usage mode** – When this bit is set high (1), the board is operating with a reduced network transmission bandwidth of approximately 8%. This prevents the node from occupying the full network bandwidth. The PCI interface will automatically be slowed down if the host attempts to write too much data. This mode is enabled by setting switch S1 position 2 in the ON position. This setting is normally OFF. This bit is read-only.
Bits 17 and 16	**Offset 1 and Offset 0** – When the host PCI system writes to the onboard memory and initiates a packet over the network, Offset 1 and Offset 0 will apply an offset to the network address as it is transmitted over the network. The offset does not appear on local access to the memory, and the offset does not alter network packets as they pass through the board. Offset 1 and Offset 0 provide four possible binary increments of 64 MB each through the 256 MB network address range. When the address and offset exceeds the 256 MB network address range, the address bits beyond 256 MB will be truncated. This causes the write to wrap around into a lower memory location. Offset 1 and Offset 0’s bits correspond to the network address bits A27 and A26 respectively.

Offset 1	Offset 0	Offset applied
0	0	0
0	1	0x400000
1	0	0x800000
1	1	0xC00000

Bits 15 through 08	**Reserved** – These bits are reserved.
Bit 07	**TX FIFO Empty** – A logic high (1) indicates the TX FIFO is currently empty. This bit provides immediate status only (not latched) and is read-only.
Bit 06	**TX FIFO Almost Full** – A logic high (1) indicates the TX FIFO is currently almost full. This bit provides immediate status only (not latched) and is read-only. Periodic assertion of this bit is normal.
Bit 05	**Latched RX FIFO Full** – A logic high (1) indicates the RX FIFO has experienced a full condition at least once. This bit is read-only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.
Bit 04	**Latched RX FIFO Almost Full** – A logic high (1) indicates the RX FIFO is operating at the maximum acceptable rate. Under normal operating conditions, this event should not occur. This bit is read-only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.
Bit 03	**Latched Sync Loss** – A logic high (1) indicates the receiver circuitry has detected the loss of a valid signal at least once since the last time the flag has been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. A logic high may indicate the receiver's link was intentionally or unintentionally disconnected.
Bit 02	**RX Signal Detect** – A logic high (1) indicates the board receiver is currently detecting light. This bit provides immediate status only (not latched) and is read-only. The status of this bit is also indicated by the Signal Detect LED.
Bit 01	**Latched Bad Data** – A logic high (1) indicates the board receiver circuit has detected bad (invalid) data packets at least once since power up or since the flag had previously been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. This bit is read-only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.
Bit 00	**Latched Own Data** – A logic high (1) indicates the board has detected the return of its own data packet at least once since this bit has previously been cleared. This bit serves as an indicator that the link is intact. The Own Data bit should be set any time a write to the onboard memory occurs or any time a network interrupt is initiated. This bit is both read and write accessible. The status of this bit is indicated by the Own Data LED.

10.8.3.6 Local Interrupt Status Register (LISR) [BAR2.0x10]

The *ibaFOB-R* board contains a number of sources for the interrupt.

The second tier of interrupts are logically "ORed" together into a single interrupt called the Local Interrupt. The Local Interrupt is, in turn, controlled by Bit 11 of the Local Configuration register (INTCSR at BAR0.0x68).

The local interrupts are controlled by two RFM registers: LISR and LIER.

Local Interrupt Status Register

This is a 32-bit register containing a group of interrupt status bits. The LIER contains a corresponding group of enables. Before any local interrupt can cause an interrupt on the Local Interrupt line, the Status Bit, its Enable and the Global Enable must be asserted.

Local Interrupt Status Register

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Auto Clear Flag	Global Interrupt Enable	Reserved	Reserved	Sync Loss	RX FIFO Full	RX FIFO Almost Full	Bad Data
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Pending Net. Int. 4	Rogue Packet Fault	TX FIFO Full	Reserved	Reset Node Request	Pending Net. Int. 3	Pending Net. Int. 2	Pending Net. Int. 1

Local Interrupt Status Register Bit Definitions

Bit 15	**Auto Clear Flag** – This bit is a read-only status indicator of the corresponding bit in the LIER Register. When this bit is high (1), the Global Interrupt Enable (Bit 14) will automatically be cleared as this register (LISR) is being read. Clearing the Global Interrupt Enable de-asserts the Local Interrupt and, in turn, releases the PCI Interrupt.
Bit 14	**Global Interrupt Enable** – This bit must be set high (1) in addition to any interrupt flag and its associated enable bit in the LIER before the Local Interrupt line is asserted and a PCI interrupt can result. If the Auto Clear enable bit in the LIER is set high (1), the Global Interrupt Enable bit will automatically be cleared as this register (LISR) is being read. This allows for a single read-modify-write operation to service the local interrupts. All following bits are set and latched when an event occurs. Once set, it must be cleared by writing a zero to that bit location.
Bit 11	**Sync Loss** – When this bit is high (1), the receiver circuit has lost synchronization with the incoming signal one or more times. The assertion of this bit usually indicates the receiver link was or is disconnected, either intentionally or unintentionally, and data may have been lost. This event will also occur if the upstream node tied to the receiver is powered off or is disabled.

Bit 10	**RX FIFO Full** – When this bit is high (1), the RX FIFO has been full one or more times. This is a fault condition and data may have been lost.
Bit 09	**RX FIFO Almost Full** – When this bit is high (1), the RX FIFO has been almost full one or more times. The assertion of this bit indicates the receiver circuit is operating at maximum capacity. If it does occur, the host should temporarily suspend all write and read operations to the board.
Bit 08	**Bad Data** – When this bit is high (1), the receiver circuit has detected invalid data packets one or more times.
Bit 07	**Pending Net. Int. 4** – When this bit is high (1), one or more type 4 network interrupts have been received. Interrupt Sender Data and Node ID can be obtained from registers ISD4 and SID4 respectively.
Bit 06	**Rogue Packet Fault** – When this bit is set high (1), the board is operating as either Rogue Master 1 or 0 and has detected and removed a rogue packet.
Bit 05	**TX FIFO Full** - When this bit is high (1), the TX FIFO has been full one or more times. This is a fault condition and data may have been lost.
Bit 03	**Reset Node Request** – When this bit is high (1), another node on the network has requested that the host would reset this board. The *ibaFOB-R* board does not reset itself automatically.
Bit 02	**Pending Net. Int. 3** – When this bit is high (1), one or more type 3 network interrupts have been received. Interrupt Sender Data and Node ID can be obtained from registers ISD3 and SID3 respectively.
Bit 01	**Pending Net. Int. 2** – When this bit is high (1), one or more type 2 network interrupts have been received. Interrupt Sender Data and Node ID can be obtained from registers ISD2 and SID2 respectively.
Bit 00	**Pending Net. Int. 1** – When this bit is high (1), one or more type 1 network interrupts have been received. Interrupt Sender Data and Node ID can be obtained from registers ISD1 and SID1 respectively.

10.8.3.7 Local Interrupt Enable Register (LIER) [BAR2.0x14]

A 32-bit register containing a group of interrupt enable bits corresponding to the status bits in LISR.

Local Interrupt Enable Register

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Auto Clear Flag	Global Interrupt Enable	Reserved	Reserved	Sync Loss	RX FIFO Full	RX FIFO Almost Full	Bad Data
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Pending Net. Int. 4	Rogue Packet Fault	TX FIFO Full	Reserved	Reset Node Request	Pending Net. Int. 3	Pending Net. Int. 2	Pending Net. Int. 1

10.8.3.8 Network Target Data Register (NTD) [BAR2.0x18]

A 32-bit register containing the data associated with one of the four network interrupts that will be sent to the target (destination) node. Writing data to this register does not initiate the actual interrupt; only writing to the Network Interrupt Command (NIC) register will do so. The NTD register is both read and write accessible.

10.8.3.9 Network Target Node Register (NTN) [BAR2.0x1C]

An 8-bit register containing the node ID of the target (destination) node. Writing to the NTN register does not initiate the actual network interrupt. This register is both read and write accessible. The NTN register can be written or read with the Network Interrupt Command Register as a single 16-bit word.

10.8.3.10 Network Interrupt Command Register (NIC) [BAR2.0x1D]

An 8-bit register containing a four-bit code that defines the type of network interrupt issued. See the table below for a definition of the possible codes. The NIC is both read and write accessible. Only writing to the NIC register will initiate the network interrupt. The network interrupt is transmitted in order following after all previously written data.

Network Interrupt Command Register

NIC [3,2,1,0]	Function
X000	Reset Node Request (sets LISR Bit 3 only, the user application must perform the actual reset)
X001	Network Interrupt 1 (stored in a FIFO at the receiving node)
X010	Network Interrupt 2 (stored in a FIFO at the receiving node)
X011	Network Interrupt 3 (stored in a FIFO at the receiving node)
X100	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X101	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X110	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X111	Network Interrupt 4 (stored in a FIFO at the receiving node)
1XXX	Global enable. Send to all nodes regardless of NTN Register

The NTD, NTN and the NIC registers described above are used to generate network interrupts. Four pairs of registers described below are involved with receiving those network interrupts.

10.8.3.11 Interrupt 1 Sender Data FIFO (ISD1) [BAR2.0x20]

A 32-bit FIFO containing up to 127 DWords of data, which has been sent to this node in type 1 network interrupt packets. The function of the 32 bits of data is user defined.

The ISD1 is a FIFO, but it is coupled and slaved to the companion FIFO SID1. Essentially, there is only one address pointer for both FIFOs and that pointer is only affected by access to the SID1 FIFO. For this reason, each location within the data (ISD1) FIFO can be read multiple times without incrementing the address pointer, while reading the companion SID1 FIFO increments the pointer for both FIFOs. For this same reason, the user must read the data (ISD1) before the Sender ID (SID1) or the corresponding data will be lost.

10.8.3.12 Interrupt 1 Sender ID FIFO (SID1) [BAR2.0x24]

An 8-bit FIFO containing the Node ID corresponding to the data in ISD1. Each time a node issues a network interrupt, it includes its own node ID as part of the packet. At each other network node, the interrupt packet is evaluated. If the network interrupt is directed to that node, and if the network interrupt is of type 1, then the sender's node ID is stored in a FIFO called the Interrupt 1 Sender ID FIFO or SID1. Like any normal FIFO, each time the SID1 is read, the FIFO address pointer automatically increments to the next location in the FIFO. Therefore, each sender ID can only be read once from the SID1 FIFO. Writing to the SID1 register flushes the contents of the complete FIFO. Note that the value of zero is NOT a true indicator that the FIFO is empty since zero is also a valid node ID. To see if network interrupts are pending, examine bits 07, 02, 01 and 00 in the LISR register.

10.8.3.13 Interrupt 2 Sender Data FIFO (ISD2) [BAR2.0x28]

A 32-bit FIFO functioning just like ISD1 but for type 2 network interrupts.

10.8.3.14 Interrupt 2 Sender ID FIFO (SID2) [BAR2.0x2C]

A 8-bit FIFO functioning just like SID1 but for type 2 network interrupts.

10.8.3.15 Interrupt 3 Sender Data FIFO (ISD3) [BAR2.0x30]

A 32-bit FIFO functioning just like ISD1 but for type 3 network interrupts.

10.8.3.16 Interrupt 3 Sender ID FIFO (SID3) [BAR2.0x34]

A 8-bit FIFO functioning just like SID1 but for type 3 network interrupts.

10.8.3.17 Interrupt 4 Sender Data FIFO (ISD4) [BAR2.0x38]

A 32-bit FIFO functioning just like ISD1 but for type 4 network interrupts.

10.8.3.18 Interrupt 4 Sender ID FIFO (SID4) [BAR2.0x3C]

A 8-bit FIFO functioning just like SID1 but for type 4 network interrupts.

10.8.3.19 Link Load (RXU) [BAR2.0x64]

A 16-bit read-only register giving an indication how much relative bandwidth is being occupied by all traffic on the fiber optic link. Unit is 1/256 of a percent (e.g. 256=1%)

10.8.3.20 Own TX Load (TXU) [BAR2.0x66]

A 16-bit read-only register giving an indication how much relative bandwidth is being used by all our own generated traffic on the fiber optic link. Unit is 1/256 of a percent.

10.8.3.21 FPGA status information (FSTAT) [BAR2.0x70]

FPGA status information

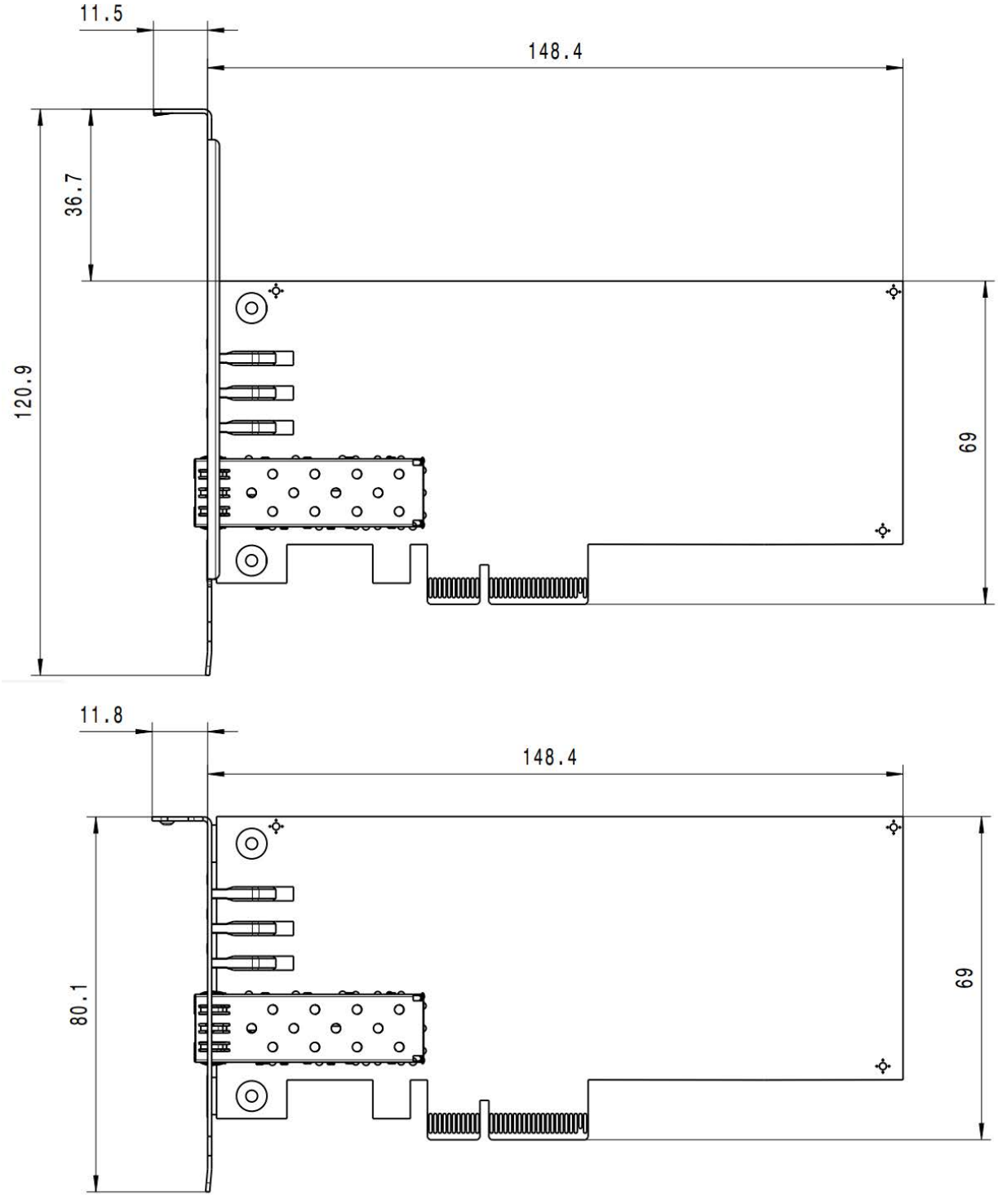
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Major Version number (BCD encoded)							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Minor Version number (BCD encoded)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Build Version number (Decimal encoded)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
FW Version Running 0: User 1: Golden	PCIe speed 0: Gen1 1: Gen2	PCB Revision Number		Reserved	Reserved	PCI link width 00 : x1 01: x2	

11 Technical data

Manufacturer	iba AG, Germany
Order no.	11.112620
Description	Reflective Memory board ibaFOB-R
Format / size	PCI Express board, low profile, x4 form factor ■ Mechanical x4 slot needed ■ Electrical up to 2 lanes used (x2) ■ Gen1 (2.5 GT/s) and Gen2 (5 GT/s) supported
Fastest sampling time in ibaPDA	1 ms
Data transmission rate	2.125 Gbaud bidirectional data link
Connection technology	SFP with Duplex LC connector
	Up to 500 m on 50/125 µm multimode fiber, 300 m on 62.5/125 µm multimode fiber
Further interfaces, operating and indicating elements	
Switches S1 and S2	See chapter ↗ *Configuration*, page 18
Indicators	3 LEDs for device status
Operating and environmental conditions	
Humidity class (DIN 40040)	F, no condensation
Protection type	IP20
Temperature range	
Operation	32 °F ... 122 °F (0 °C ... 50 °C)
Storage and transport	-13 °F ... 158 °F (-25 °C ... 70 °C)
Cooling	Passive
Power supply	Via PCIe slot (12 V/3.3 V)
Power consumption	3 W (typical)
Certifications / standards	EMC: IEC 61326-1 FCC part 15 class A
Dimensions	
Low profile bracket	80.1 mm x 148.4 mm
Standard bracket	120.9 mm x 148.4 mm
Weight / incl. packaging	0.21 lb (93 g) / 0.39 lb (175 g)

11.1 Dimensions

ibaFOB-R with standard bracket (figure above) and low profile bracket (figure below).



Dimensions in millimeter (mm)

12 Support and contact

Support

Phone: +49 911 97282-14

Email: support@iba-ag.com

Note

If you need support for software products, please state the number of the license container. For hardware products, please have the serial number of the device ready.

Contact

Headquarters

iba AG
Koenigswarterstrasse 44
90762 Fuerth
Germany

Phone: +49 911 97282-0

Email: iba@iba-ag.com

Mailing address

iba AG
Postbox 1828
D-90708 Fuerth, Germany

Delivery address

iba AG
Gebhardtstrasse 10
90762 Fuerth, Germany

Regional and Worldwide

For contact data of your regional iba office or representative please refer to our web site:

www.iba-ag.com